A 100 KW SOLID STATE COAXIAL SWITCH

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ABSTRACT

A high power L-band PIN diode switch is described. The design uses 16 high voltage PIN diodes in a novel coaxial structure. The switch has been tested to 100 kW peak power. Insertion loss is less than 0.25 dB and isolation is greater than 25 dB across 14% bandwidth.

INTRODUCTION

This paper describes the development of a high power solid state coaxial SPST switch for L-band. It is designed as part of the antenna sub-system of a long-range surveillance Westinghouse radar. In this system, transmitter power to certain azimuth rows of the antenna is reduced for the so-called high beam mode. The RF power is not perfectly nulled because of phase differences in the manifold. The switch described here provides an additional 25 dB (minimum) attenuation for this mode. In the low loss state, the switch has been shown to pass 100 kW peak, 0.001 duty pulses across 1.215-1.4 GHz. In the high attenuation state, it provides a minimum 25 dB attenuation for power levels up to 60 kW peak, and it must survive up to 100 kW peak in the unlikely event of an antenna fault. Switching time is required to be less than 10 μsec. Hot switching is not required.

This switch incorporates several novel design features. The PIN diodes in shunt across the line are grounded to the outer conductor. Bias is passed to the diodes via a simple feedthru and RF choke. The PIN diodes are a high voltage type normally used for much lower frequencies. They are series resonated for high isolation in the ON state by ceramic capacitors at the center conductor. This allows the center conductor to be DC grounded, and eliminates the complex chokes normally required for high power PIN diode switches.

COAXIAL DESIGN

Basic requirements for the switch design are low insertion loss, 100 kW peak rf power handling, ease of fabrication, and long life time reliable operation. Electrical requirements for the high power switch are presented in Table I.

Table I. Electrical Performance for the High Power Switch.

Performance	Limits
Frequency Range	1215 MHz to 1400 MHz
VSWR	1.3:1 Max (50 ohms)
Isolation	25 dB Min (forward bias)
Insertion Loss	0.4 dB Max (reverse bias)
Switching speed	10 Microseconds Max
Peak Power Handling	100 kW (reverse bias) 60 kW (forward bias)
Duty cycle	0.001
Pulsewidth	3 Microseconds
Input/Output	1-5/8 Inch EIA Connectors
Device Configuration	SPST

The mechanical configuration of the switch in 1 5/8 inch EIA coaxial transmission line is shown in figure 1. PIN diodes are shunted between the center and outer conductors in a multi-spoke arrangement forming two diode planes, with four spokes per diode plane. Each spoke contains a metal mount with cascaded dual diode assembly, a high power ceramic capacitor, an RFI filter, and two bias chokes. The threaded stud mount (figure 2) acts as a heat sink for the dual PIN assembly and can be conveniently screwed into the outer conductor housing after being fully assembled separately. The cascaded dual diode assembly provides a voltage breakdown (V_{BR}) greater than 3000 Volts and reduces the net shunt diode capacitance across the coaxial line in the reverse bias mode, resulting in low insertion loss.

Ceramic capacitors insulate the center conductor from the dc bias which is returned to the outer conductor through high impedance wirewound chokes. This arrangement eliminates the need for series dc blocking capacitors in the coaxial line at the input and output ports. The ceramic capacitor value is chosen to series resonate the diode package inductance for maximum isolation in the forward bias mode. Very high RF voltages exist across the capacitors in both ON and OFF states. When the diodes are OFF, the full transmitter power is

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present across the net capacitance of the diodes and the series capacitor. When the diodes are ON, a peak RF current of about 12 A flowing through the effective short circuit is sufficient to develop nearly 1 kV across the capacitor. In addition, the ceramic material helps to heat sink the PIN diodes to the center conductor. The alumina capacitor disks are soldered to goldplated copper plates mounted on the center conductor. The edges of the exposed capacitor electrode are coated with a proprietary arc-resistant epoxy to prevent arcing during high power operation.

The aluminum center conductor is gold plated for solderability, corrosion protection and to minimize resistance. It is mechanically supported within the outer conductor housing by the input/output anchor insulator coaxial connectors. Eight dual diode spoke assemblies are fabricated in a large diameter threaded aluminum stud mount (figure 1B). Each mount consists of an RFI filter, a bias choke, two cascaded PIN diodes, and a dc return choke. A beryllium copper spring washer is placed on top of the capacitor plate to make rf contact with the PIN diodes. The tuning stub center conductor and sliding short installed in each diode plane help to mechanically stabilize the main center conductor.

PIN DIODES

Presently, the high power PIN diode are available only in a relatively large hermetic ceramic package (MA 1027 package) designed primarily for HF (~ 100 MHz) applications. We have extended their operational range to L-band by using cascaded diodes and the ceramic capacitor tuning.

In the reverse bias mode, the 100 kW peak power handling requirement was met by selecting PIN diodes with reverse breakdown voltages greater than the sum of the maximum peak rf line voltage (V_{rf}) and the reverse dc bias voltage (V_{DC}). The PIN diodes were mounted in a low impedance (12 ohm) section to reduce the RF line voltage to less than 1550 V. The reverse DC bias voltage was selected on the basis of minimum rf distortion criteria [1]. The distortion in a switch is inversely portional to the rf signal frequency, the duty cycle, and the I-layer thickness, and directly proportional to the peak rf voltage. The minimum reverse bias voltage V_{DC} required for minimum distortion with two diodes in series was computed to be 46.4 V. Therefore, a cascaded dual diode assembly with V_{BR} > 3000 V was selected to handle 100 kW peak power with 200 volts reverse bias.

The forward biased power handling requirement of 60 kW was met by using PIN diodes having 0.25 ohm forward resistance in each of the four spokes [2]. Diodes with an I-layer width of 7 mils, large junction area (3.0 pf), and low thermal impedance (2°C/W) were selected to limit the junction temperature to less than 150°C at 60°C ambient. Two diode planes spaced $\lambda/4$ apart resulted in 30 dB minimum isolation across 1200 to 1400 MHz. Table II shows the high power PIN diode parameters selected to meet the electrical requirements in Table I.

Table II. PIN diode Parameters

Parameters	Values
Junction Capacitance (-100 V),	3 pf max
Forward Resistance (@ 100 mA)	0.25 ohm max
Reverse Bias Voltage (V_{BR})	> 1500 volts
Reversations Parallel Resistance	10 K ohm typ
Package Inductance	2.0 nH
Package Capacitance	0.45 pF typ
Thermal Impedance	2°C/Watt typ
I-layer thickness	7 Milli-inch
Minority Carrier Lifetime	10 μsec

The impedance of the transformer section of the coaxial line was optimized to maximize isolation in the operational frequency range while reducing the peak voltage to a safe level for the PIN diodes.

An electrical schematic is shown in figure 3. In the reverse bias mode, the cascaded PINs and ceramic capacitances are parallel resonated by a shunt inductive 100 ohm shorted stub. The theoretical minimum insertion loss and return loss of the reverse biased switch were 0.18 dB and 26 dB respectively across 1200 MHz to 1400 MHz. In the forward bias mode, the inductance of the PIN diode assembly was series resonated by the alumina capacitors to achieve 34 dB minimum isolation with 0.25 ohm forward resistance of the PIN diodes.

MEASURED PERFORMANCE

Low level insertion loss and return loss measurements were made over 1215 MHz to 1400 MHz using an HP 8757 magnitude analyzer, and are shown in figure 4. Maximum insertion loss with -200 V bias is 0.22 dB and the minimum return loss is 18 dB. Low level isolation for the switch "ON" mode is 27 dB minimum, as shown in figure 5. Peak-to-peak deviations for low level insertion loss and return loss over -40°C to +60°C in the passband were found to be 0.08 dB and 0.59 dB respectively. Switching times from ON to OFF and OFF to ON conditions were measured to be 5 microseconds and 10 microseconds respectively.

High power measurements were made at 1.3 GHz using 100 kW peak incident rf power at 0.0009 duty cycle and 3.0 microseconds pulsewidth. In the reverse bias mode with -200 V dc bias, the input power was varied from zero to 100 kW peak power. Power meters at the input and output ports of the test switch were used to determine any variations in insertion loss during the test. Input and output rf signal waveforms were monitored on an

oscilloscope during the test. There were no indications of distortion, arcing or insertion loss variations during the high power testing of the device. In the forward bias mode, the PIN diodes were biased with 640 mA dc current (total) and the leakage (output) power amplitude and waveforms were monitored while varying the incident peak rf power from zero to 60 kW. A leakage level of 59 W was measured at 60 kW peak rf incident power, giving an isolation of 30 dB which equaled the measured low level isolation at 1.3 GHz. The device was tested up to 80 kW peak incident power level without any fault.

DRIVER

The driver circuit supplies the required forward bias current of 640 mA and the reverse bias voltage of -200 V to the 16 PIN diodes, which are in parallel as far as bias is concerned. The prime power available is 20 VDC. An internal DC-DC converter produces the -200 V for reverse bias. The required switching time is 10 μsec, at an effective repetition rate of about 500 Hz. Built-in fault detection circuitry can detect shorted or open PIN diodes or loss of reverse bias. Command signals to the switch are through RS-422 logic.

Forward bias is supplied to the PIN diodes through a high voltage P-channel MOSFET power transistor. PIN diode current is fed thru a sensing resitor, and a feedback circuit to the FET gate maintains the bias at 640 mA over all normal supply voltage and temperature variations.

Reverse bias is supplied thru an N-channel MOSFET which is switched in complement with the forward bias FET.

Fault detection circuitry consists of optically isolated LEDs in the forward and reverse bias drivers and associated logic. Should the bias current fall below a preset level in the forward bias state, the decrease in output from the optocoupler is sensed and the logic circuit sends a fault signal to the main processor. In case of a shorted PIN, current flowing through the optocoupler LED in the reverse bias driver is sensed, causing a fault signal to be sent. The fault detection circuitry is gated to ignore the normal PIN and choke discharge currents flowing at the end of each switch cycle.

The DC-DC converter produces -200 V for reverse bias operation. Normally, negligible current would flow in reverse biased PIN diodes, but the current needed to charge and discharge the RF feedthru capacitors requires an average of about 10 mA from this supply. The output of the DC-DC converter is also continuously monitored by the fault detection circuitry.

The DC-DC converter and driver are in a housing attached to the RF assembly, as shown in figure 6.

SUMMARY

We have described a high power PIN diode coaxial switch for L-band. The switch incorporates unique design features that allow use of high voltage PIN diodes which were originally designed for much lower frequencies. Insertion loss is less than 0.25 dB and isolation is greater than 25 dB. The switch can handle 100 kW peak power in both states. An integral driver produces switching times under 10 μsec and includes built-in fault detection.

REFERENCES

1. Hiller, G. and Caverly, R., "The Reverse Bias Requirement for PIN Diodes in High Power Switches and Phase Shifters", 1990 IEEE MTT-S International Microwave Symposium Digest, May, 1990, pp. 1321-1324.
2. Dominick, F., "How much pulsed power can a PIN diode handle?", Microwaves, February, 1976, pp. 54-59.

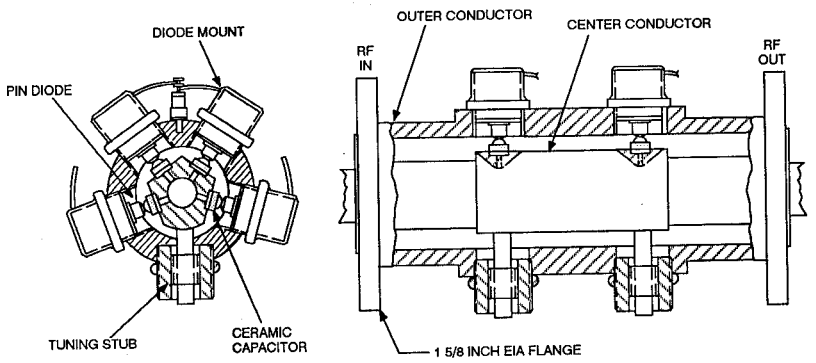

Figure 1. Mechanical Configuration of RF Housing with Diode Mounts and Ceramic Capacitors

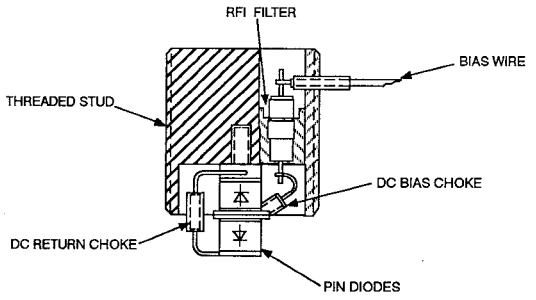

Figure 2. Diode Mount with Cascaded PIN Diodes

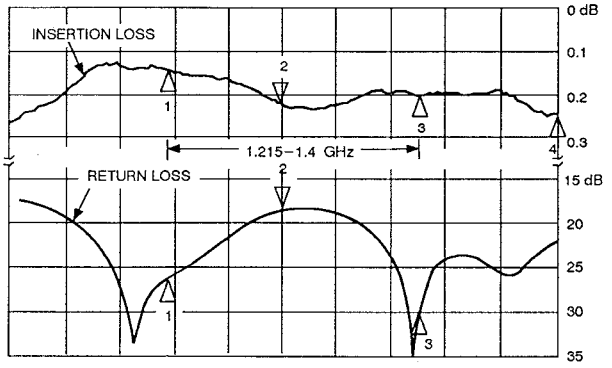

Figure 4. Low Level Insertion Loss and Return Loss Measurements with -200V Bias

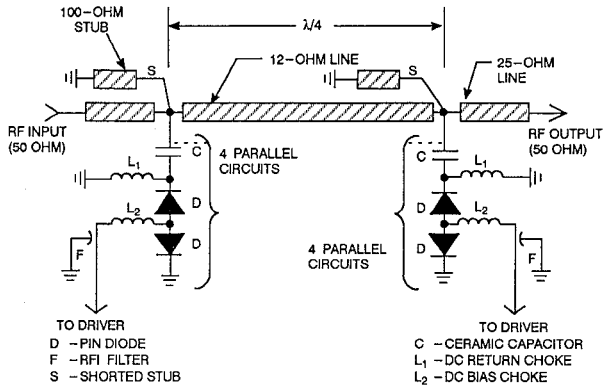

Figure 3. Electrical Schematic of the High Power Switch

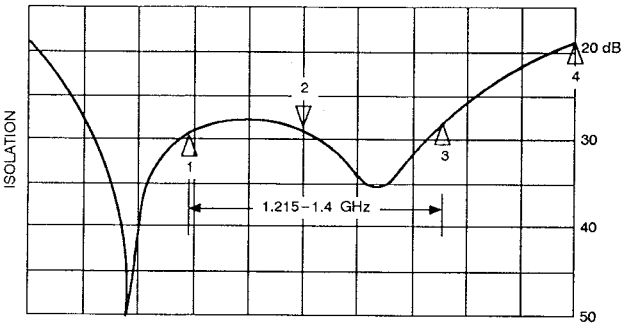

Figure 5. Low Level Isolation Measurements with 640 mA Forward Bias

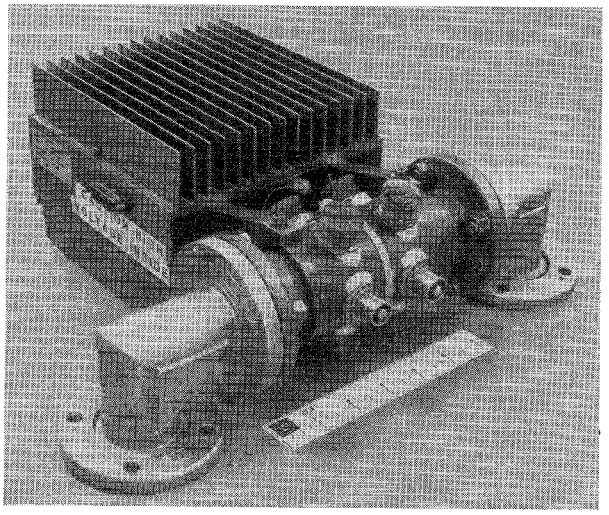

Figure 6. Photograph of the Switch Showing RF and Driver Housings